COTS-BASED MODULAR BLDC POWER STAGE USING GaN-FETS FOR ROBOTIC SPACE APPLICATIONS

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***Abstract*—Within this paper we present the design and implementation of a modular commercial off the shelf (COTS)-based brush less direct current (BLDC) power stage using gallium nitride - field effect transistors (GaN-FETs). Possible application scenarios are small mobile systems for lunar application with short and medium envisaged mission lifetime. We are giving details in the design process of the power stage and component selection process. Furthermore, mitigation techniques for radiation environment, redundancy and special electrical design considerations are covered. Detailed insights in development, design, and production of the power stage, are presented and next steps for technology readiness level (TRL) increase. The described results are based on the DFKI's outcome of the project iCOTS[1] which ended in July 2023.**

***Index Terms*—BLDC, GaN-FET, COTS, Space Robotics**

I. Introduction and Related Work

With the increasing interest in the exploration of celestial bodies, such as the lunar surface, or on orbit servicing [1] the demands on robotic systems for future space missions are constantly increasing in terms of performance and compactness. In this context the actuators and the associated motor electronics play a key role in robotic systems. [2] The radiation environment poses particular challenges for the electronic design and component selection. The objective of the present work was the development of a COTS-based BLDC power stage using GaN-FETs for future robotic systems with short and medium mission lifetime in lunar environment. The power stage is designed for a nominal power of up to 80 W at 28 V. Five to ten times higher peak performances are conceivable due to the derating of critical components. Parts of the presented electronic design are based on experience and proven approaches from previous research [3] [4]

[1]https://robotik.dfki-bremen.de/en/research/projects/icots

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II. Design Approach

A. Module Design and Backplane Approach

The design of the BLDC power stage follows a modular backplane approach enabling flexibility during system design as this is a technology demonstration. An assembly of the described electronic configuration is depicted in Figure 1. Further configurations, for example leave out the redundant power stage to save space and mass are conceivable. Alternative configurations are possible by simply exchange the backplane. In the present configuration the power stage consists of:

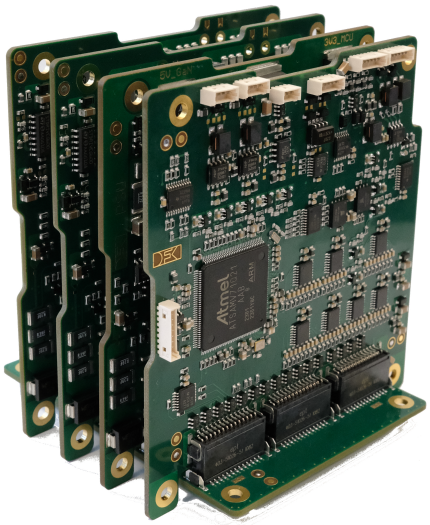

Fig. 1. Assembled modular BLDC power stage electronic consisting of the backplane an the connected MCU board, PSU board, and two cold redundant BLDC power stages.

- A backplane providing communication, discrete signals, and power lanes to all electronic boards,
- an MCU board implementing the motor control, communication and sensor interfaces,

- a PSU implementing intermediate voltage regulation (5 V, 3.3 V)for sensors, gate drivers etc.,
- a cold dual modular redundancy (DMR) BLDC power stage unit using GaN-FET.

B. Design Process and Component Selection

The design process followed within the present development is described in Figure 2 in its individual steps. This development followed a COTS-based approach envisaged for medium acceptable risk for short and medium lunar mission duration.

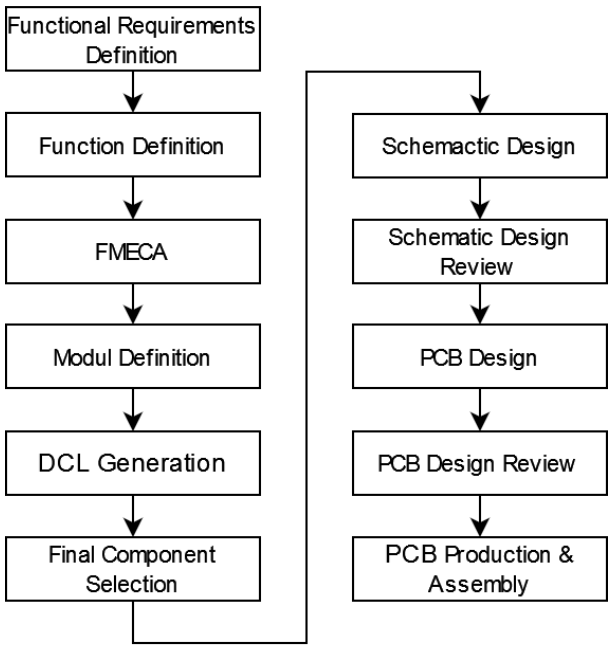

Fig. 2. The individual steps of the component selection and design process start from the definition of the functional requirements through the final selection of the components and finally to the design and manufacture of the electronics.

First of all the functional requirements were defined followed by a function definition. We have carried out a failure modes criticality and effects analysis (FMECA) to characterize possible failure modes of the power stage and identify most critical components. Following components were identified as most critical for functioning of the power stage as all of them could cause a fatal failure:

- GaN-FETs
- GaN-FET Half-Bridge Driver
- latching current limiter (LCL)
- MCU
- magnetoresistive random access memory (MRAM)

Next the modules were defined and the individual functions were mapped to the modules under the condition of a modular design. With the identified critical functions as basis a declared component list (DCL) was generated. The DCL was used to identify the critical components for which radiation tolerance could not be confirmed by design or test. In case of the GaN-FETs, the half bridge drivers, and the LCL two candidates each were selected to be foreseen for future radiation test campaign to characterize the behaviour of the selected components in heavy ion environment. We selected the COTS components to be used, as far as possible, according following selection criteria:

- Package processability,
- derating inline with ECSS-Q-ST-30-11C Rev.2 (Derating - EEE components) [5]) or higher,
- automotive rating (AEC-Q 100) preferred over industrial temperature range ($-40\,°C$ to $+85\,°C$),
- International Traffic in Arms Regulations (ITAR) free components

Following the selection of the most critical components is discussed.

a) GaN-FETs: Two manufacturers currently offer GaN-FETs on the market that are specifically designed for low voltages. These are gallium nitride (GaN)-Systems (Canada) and Efficient Power Conversion Corporation (EPC - USA). Potential candidates could be found at both companies.

GaN-Systems has a series of $100\,V$ GaN-FETs with similar parameters than EPC. We chose a $100\,Vds$, $7\,m\Omega$ and $8\,nC$ typical total gate charge type with the GS61008 series. We selected the GS61008P [6] (dissipation into the PCB).

Within the X-Joint [3] [4] and SEARCH-EPS [7] development, we already used EPC GaN-FETs and are familiar with some of their so-called "die-size" packages and the potential PCB assembly challenges. We decided to choose a type in ball grid array (BGA) package with 1mm pitch instead of a passivized die with $0.4\,mm$ or $0.5\,mm$ pitch solder bars. Here we chose the EPC2029 [8] with $80\,Vds$, $3.2\,m\Omega$ RDS(on) and $13\,nC$ typical total gate charge.

b) GaN-FET driver: Since GaN-FET in contrast to Si-field effect transistors (FETs), have a low gate voltages of $5\,V$ to maximum $6\,V$, the typical SiFET gate drivers are not suitable. Si-FET gate drivers usually have a shutdown threshold of $\leq 10\,V$ to prevent the Si-FETs from linear mode operation due to a gate voltage that would be too low for low ohmic mode. However, this shutdown threshold is already above the allowed maximum gate-to-source voltage of the GaN-FETs to be used. Therefore, special drivers must be used at this point.

As first candidate, we selected STDRIVEG600 from STmicro [9]. This driver is offered in a well processable SO-16 footprint as well as bare die. We chose the SO-16 variant.

As an alternative, we selected the LM5113-Q1 driver from Texas Instrument [10]. Within the X-Joint development [3] [4] we have already been able to gain experiences with this component. We selected LM5113-Q1 in plastic small-outline no-lead package (WSON) package as candidate because of its in X-Joint heritage.

Due to the short project runtime, we were only able to develop one variant of the power driver, so we decided to use the GaN-FET GS61008P and the STDRIVEG600 driver. This decision was made in order to prevent possible ITAR problems with the component selection from the very beginning. Nevertheless, we developed breadboards for irradiation

tests with both variants of GaN-FETs and drivers to compare them under relevant radiation environment in future.

c) LCL: Since we only use untested COTS components that can potentially latch-up, there is over current protection in the power supply in front of each function that contains complementary metal-oxide-semiconductor (CMOS). Again, we used components known from previous X-Joint development [4]. We selected two types with different current ratings. Both are based on PFETs based and deactivates itself if a current threshold is exceeded. In addition to their protective role, these can also be used for an extended low power mode by completely de-energizing unused circuit parts. Following the selected LCLs:

- FPF2006 from OnSemi [11] with $100\,mA$ max. threshold.
- FPF2106 from OnSemi [12] with $400\,mA$ max. threshold.

d) MCU: As MCU we selected a Cortex-M7 ARM-based SAMV71Q21-AAB from Microchip (formerly Atmel) [13]. This is used in automotive AEC-Q100 Grade 2 ($-40\,°C$ to $+105\,°C$) COTS. It offers all required peripherals like dual CAN-BUS controller, 12-bit analog-to-digital converter (ADC), pulse-width modulation (PWM) timer, enough I/Os and integrated memory. This MCU is also in focus of space-components because it is available as a high-reliability version (SAMV71Q21-ET [14]) and radiation-tolerant version (SAMV71Q21-RT [15]). The SAMV71Q21-AAB is an ideal low-cost evaluation platform and software compatible with the ET and RT version. With the SAMRH707 [16], a comparable radiation-hard version with a similar feature set is available, as well.

e) MRAM: Since the flash-cells in the MCU can be influenced by charged particles causing potential bit flips, we needed an option to keep a non influenced gold standard of the binary firmware for comparison and reprogram the MCU if required. An option could be an additional memory on the MCU board. Since we also use untested COTS components for this, this memory should be redundant as well and must have a capacity of at least the size of the MCU memory of 2048 Kbytes. To save I/Os, we used an serial peripheral interface (SPI) interface. Since industry-standard flash devices are based on the same influenceable technology as the MCUs flash, we chose MRAM. MRAM is not subject to radiation induced bit-flips as flash technology. Here we selected the MR25H40 [17] MRAM from Everspin Technologies in the automotive AEC-Q100 Grade 1 ($-40\,°C$ to $+125\,°C$) rating. As mentioned before, in redundant design including overcurrent protection circuitry for each device. In addition, each MRAM device is connected to its own dedicated SPI port of the MCU to ensure that only active devices are supplied with electrical signals.

A summary of all selected COTS components is shown in Table I.

TABLE I
SELECTED COTS COMPONENTS AND POTENTIAL ALTERNATIVES

Type	First Choice	alternative
GaN-FET	GS61008P	EPC2029
Gate-Driver	STDRIVEG600	LM5113-Q1
LCL (100 mA)	FPF2006	
LCL (400 mA)	FPF2106	
MCU	SAMV71Q21-AAB	
MRAM	MR25H40	

C. Mitigation Techniques

a) Redundancy: There are several local onboard redundancy mechanisms to increase the availability of module. On the plus side, the actual BLDC power stage unit with its relevant sensors is optionally provided in duplicate as a cold-redundant functional unit. In addition, the voltage generation via switched-mode power supply (and here specifically via COTS) is provided as a possible source of error with dual (hot or cold) redundancy.

b) Latch-up Prevention: Since CMOS COTS components can potentially generate a latchup, each functional unit (e.g. gate driver of the half-bridges) based COTS components is protected with an integrated PFET-based overcurrent protection switch. This can also be used for power management and to de-energise circuit parts that are not required. In the case of memory components, for example, the switch can also be used to experience a larger total ionizing dose (TID) without damage in powerless mode.

c) Transient Filtering: Since bipolar junction transistor (BJT)-based semiconductors can experience voltage transients due to heavy particle bombardment, appropriate filters in the form of simple RC (resistor/capacitor) are implemented at all corresponding points (low dropout regulator (LDO) outputs, current measurement circuit, etc.) as a precaution. These attenuate short-term overshoots and undershoots. In addition, the current in BJT-based integrated semiconductors is limited with a series resistor to minimise the probability of burnout due to a long-lasting transient. This also has a positive influence on the electro magnetic compatibility (EMC) behaviour of the module, since an effective first-order low-pass filter is integrated in the power supply line before each active semiconductor.

d) Additional Safety Features: The power stage has a discrete safe-torque-off (STO) signal in an electrically isolated version without a data bus.

e) Description of the protective circuits of the motor power stage: The circuit symbols of the GaN-FETs show body diodes to better illustrate the current flow. These are not physically present in GaN-FETs, in contrast to SI-FETs. However, a similar effect (third quadrant) also occurs in GaN-FETs.

Since we need a large capacitance for ripple suppression on the power section which would cause a high inrush current when the power section is switched on, a current-limiting high-side PFET was implemented. This limits the inrush current and serves as a disconnect switch to cut off the current to the power section. In addition, to protect the PFET transistor, it has a foldback current circuit to limit the power dissipation of the FET in current limiting mode (linear mode). This circuit section is completely discrete based on BJT transistors.

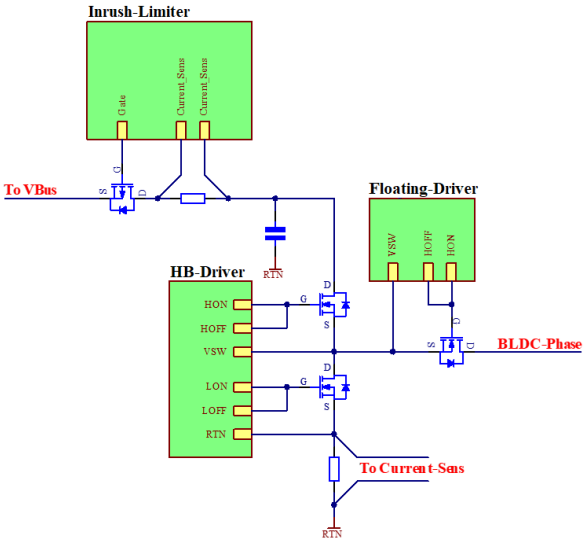

Fig. 3. BLDC fault isolation scheme. A PFET in the supply line and a additional GaN-FET per phase in serial make it possible to isolate a defective or redundant driver from a motor

The three half-bridges have an additional GaN-FET in series to the phase output with a floating high-side driver supplied by a charge pump. In normal operation, this driver is permanently set to conduction. If a fault now occurs, the PFET of the inrush limiter is switched off, which prevents a current flow from the bus to the motor driver. In addition, the serial GaN-FET in the phase is disabled, which prevents current from flowing back into the power section from the motor phases.

D. Assembly and Layout Decisions

To avoid losses during assembly and to allow manual rework as well as optical solder joint inspections, BGA was not used. In addition, if possible, components with SO (Small Outline) such as small outline integrated circuit (SOIC), thin shrink small outline package (TSSOP) or mini small outline package (MSOP) like package shapes were preferred to the "No Leads Package". Passive components below 0603 (1608 metric) were also avoided in favor of manufacturing quality.

While space saving packages were avoided, it was possible to achieve a high component packing density on the individual boards. The three different PCBs, divided into MCU, PSU and BLDC power stage, each have an identical printed circuit board (PCB) geometry of about 95.89 x 90.17 mm, contain all 8 layers. All components have been placed and routed by hand.

The PCB was assembled in-house using an automatic placement machine followed by a three-zone reflow oven. In addition to the avoidance of problematic components and our CAD footprints, which have been optimized over many years, there was no rework on the soldered assemblies. Random samples of the boards were subjected to X-ray inspection at critical points, such as the GaN-FETs, in order to examine short circuits and air inclusions in solder joints that could not be inspected optically. A summary of the project is shown in Table II.

TABLE II
SUMMARY OF LAYOUT INFORMATION

	MCU	PSU	Power Stage	Backplane
Components	660	369	574	44
Pads	1920	918	1455	457
Tracks	15720	7841	12835	1632
Vias	1104	1191	1413	609

E. MCU Board

A block diagram of the MCU board showing its main functions is depicted in Figure 4. For communication with an higher level system the MCU board is equipped with a redundant CAN with flexible data rate (CAN-FD) interface and an optional RS422 interface. As alternative it is also possible to control the module via discrete pulse-pause-modulation (PPM). For debugging an universal asynchronous receiver / transmitter (UART) and Joint Test Action Group (JTAG) interface is provided.

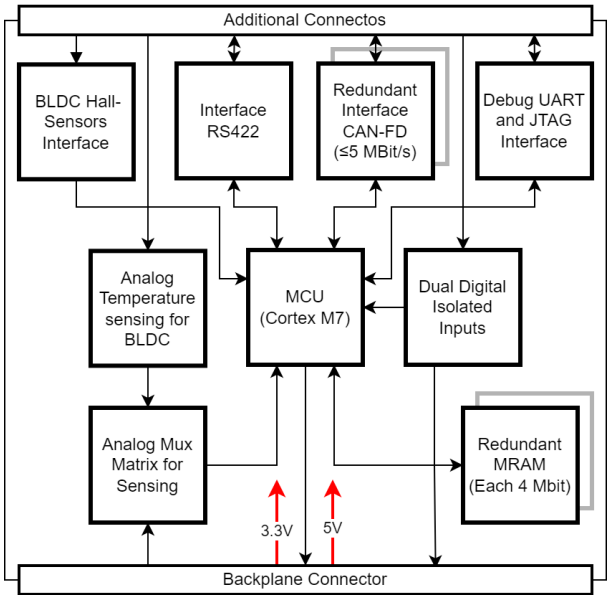

Fig. 4. The MCU board is the central unit for switching and control of the BLDC electronic and communication with a higher level system. It implements digital and analog interfaces for switching, control and sensing. Furthermore it is equipped with multiple interfaces for communication in operation and debugging. The MCU is based on a Cortex M7 with additional redundant external memory.

F. PSU

The block diagram of the PSU can be seen in Figure 5. Since a failure of the switching power supply would most likely result in a total failure of the system, it is designed redundantly and serves as a pre-regulator for LDO. The LDOs are divided by function. The 3.3 V LDO which supplies the MCU is permanently switched on. The LDOs for 5 V loads like interface or the GaN-FET drivers can be activated by the MCU.

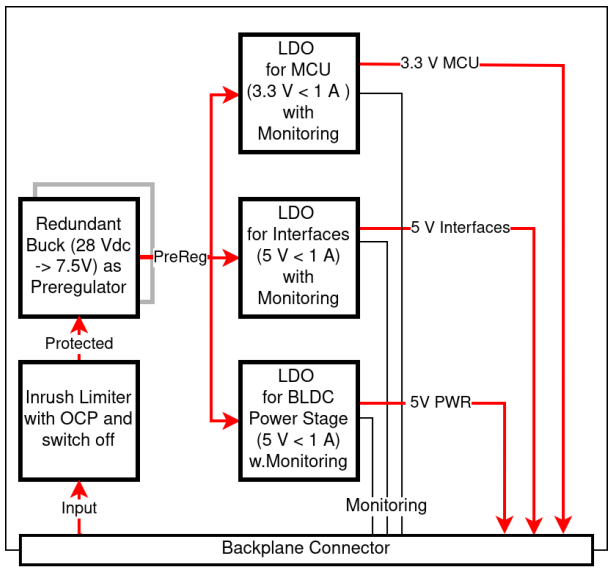

Fig. 5. The PSU board is directly connected to the $28\,Vdc$. It has an inrush current limiter that can also serve as a disconnector. Two redundant switching power supplies (buck / step-down topology) in hot or cold redundancy (user-defined) serve as pre-regulators and generate approximately $7.5\,V$ output voltage from the $28\,Vdc$. These $7.5\,V$ are converted via LDO to 1x $3.3\,V$ (for the MCU) and 2x $5\,V$ (for the interfaces such as CAN bus, and RS422 and separately for the power output stage).

G. BLDC Power Stage

In addition to the actual half-bridge drivers for the three BLDC-phases, the BLDC power stage boards, seen under Figure 6 also includes inrush limiters, which also serve as power-disconnectors, EMC-optimized filters for common mode and differential mode for the $28\,V$ supply voltage and LC filters in the output of each BLDC phase, bulk capacitors, and separate phase-disconnector GaN-FETs with floating gate drivers. By using the inrush limiter as a disconnect switch and the three phase disconnect switches, a BLDC power stage can be passivated by a BLDC motor.

III. Redundancy

Different redundancy mechanisms are implemented as radiation mitigation technique on board and function level. A summary of implemented redundancy mechanisms is given in Table III.

A. Redundant BLDC Power Stage

The BLDC power stage can be used in cold-redundant if required. For this purpose, it has functions such as a disconnector from the supply voltage by a current limiting P-FET circuitry as well as a third GaN-FET in the half-bridges in series to the phase output. If both FETs (in the power supply and the motor phase) are deactivated, no more current can flow into or out of the module to the motor and the BLDC power stage behaves passively. The selection of which power section is currently active is made by the local MCU or the higher-level system via command.

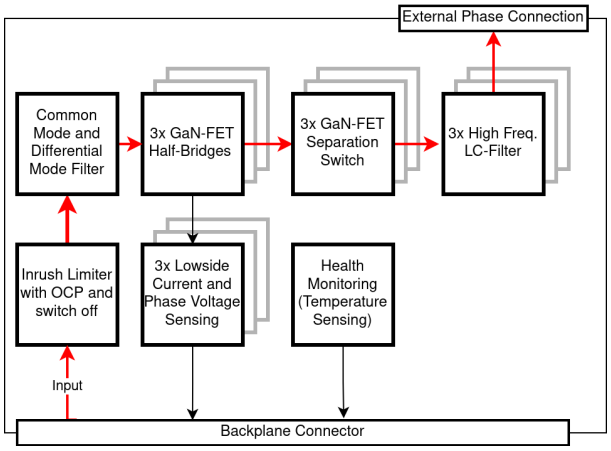

Fig. 6. The BLDC power stage board is supplied with $28\,Vdc$ via the backplane. It has an inrush limiter with over current protection and switch off functionality. The power stage implements a common-mode and differential mode filter (see section IV). Each phase can be separated and is filtered with a high frequency LC-filter. There is a low-side current and phase voltage measurement for each phase. The external phase connection is on the upper side of the PCB and is not over the backplane.

TABLE III
Summary of Redundancy Mechanisms

Function	Redundancy	Decision
BLDC Power Stage	Cold / DMR	High-Level or MCU
Step-Down Regulator	Cold or Hot / DMR	High-Level
Voltage Reference	Hot / TMR	OR-ing
Communication CAN	Cold or Hot / DMR	High-Level or MCU
ext. Memory	Cold / DMR	High-Level or MCU

B. Redundant Circuits

In the PSU, the step-down pre-regulator [18] (28 Vdc input to about 7.5 Vdc output) is designed as redundantly switching regulator to compensate a failure of one switching regulator. Each pre-regulator can be separated from the input voltage by a high-side PFET switch. Both regulators have a local output capacitor, a low ohmic resistor as transient attenuator and a power Schottky diode as logic OR in the output to block reverse currents in case of a permanent short. The pre-regulated voltages by both regulators are buffered by a large sized bulk capacitor array of 8 x $22\,\mu F$/X7R multilayer ceramic chip capacitor (MLCC) to mitigate transients, switch over and ripple reduction. BJT based PNP-LDOs [19] for the final output voltages (eg. $3.3\,V$ for the MCU or $5\,V$ for the GaN-FET gate drivers) are supplied out of this pre-regulated voltage. They also have series resistors to attenuate transients caused by radiation. The reference voltage source is also designed with triple modular redundancy (TMR) on the PSU. This is based on linear BJT-based programmable shunt references [20], which according to recently published tests by ESA (available in the ESARAD database [21]) could cause very short transients (up to $3\,\mu s$). All three references run in hot redundancy on a large output capacitance to dampen transients. However, since the large output capacity could deliver a huge amount of energy in the event of a negative tran-

sient, which could potentially destroy the transient-triggering reference. As a result, each reference has a low forward voltage Schottky diode on its output to block reverse current flow and a relatively high-resistance sense path to prevent this. The sense path references the output after the diode so that it is compensated, and the output voltage will not be reduced by the diode's forward voltage drop.

IV. Electrical Design Considerations

A. EMC Design

Various methods have been taken to ensure EMC-compliant behaviour with the modules (according to ECSS-E-ST-20-07C – Electromagnetic compatibility [22]). For example:

- A first-order LC low-pass filter with $\frac{1}{10}$ of the switching frequencies of the the BLDC power stage in order to achieve an attenuation of at least $40\,dB$.
- A common-mode filter is provided in the $28\,Vdc$ supply line on the backplane, as well as on the BLDC driver power stage, to attenuate high-frequency broadband interference.
- The bulk capacitance on the BLDC power stage is intentionally large to minimise voltage ripple on the supply bus and is based on a mixture of MLCCs of different sizes (LF: multiple $4.7\,\mu F$/X7R; intermediate: multiple $1\,\mu F$/X7R; HF: multiple $100\,nF$/X7R).
- In addition, there is a first-order HF LC filter directly at each phase output of the BLDC power stage to suppress high high-frequency interference, generated by the steep flanks of the GaN-FETs.
- Also, low-pass filters or π-filters with ferrites are provided in front of all integrated semiconductors to dampen high-frequency noise.
- Each step-down pre-regulator has a HF (HF-ferrite based) and a LF (inductor based) π-filter to minimize switching noise at the input and a shared bulky output capacitor to reduce ripple voltage. Final output voltages (single $3.3\,V$ and dual $5\,V$) are regulated by low noise BJT-based PNP low dropout voltage regulators with transient and EMC damping RC-filters and large designed capacitors to attenuate ripple.
- The PCB stack-up consists of 8 layers with dedicated power, ground, and signal layers. To minimize trace-lengths and impedance we used IPC4761 Type VII (filled and capped) through vias, directly as so called "vias in pads" of the components.
- These features still must be checked by EMI-measurement and adjusted, if necessary, as such complex modules cannot be simulated completely and many factors like the PCB-layout play an important role.

B. Inrush Limiter

To keep the inrush current pulse through the bulk capacitance as low as possible, reduce the risk of over current if the module fails, and to disconnect the BLDC power stage, a self-contained current-limiting high-side PFET with foldback-curve switch (to limit the power drop of the P-FET and thus its losses) is provided in the supply of the BLDC power stage as well as the power supply unit. It limits the current to about $10\,A$ (approx. $10\,ms$) for the BLDC driver power stage and about $5\,A$ (approx. $10\,ms$) for the power supply unit. It is self-current-limited but must be controlled externally to prevent over-heating. The BLDC power stage limiter is controlled by the MCU and the PSU by an higher arranged system

V. Conclusion

The presented electronic design, in this paper, represents a technology demonstration of a compact modular BLDC power stage using GaN-FETs for robotic space applications. Conceivable mission scenarios are small mobile systems for lunar application with short and medium envisaged mission lifetime.

The use of COTS components can be particularly beneficial for missions scenarios with short duration and higher risk acceptance compared to classical space electronics. Due the use of COTS components, more advanced electronics are available. Examples are feature-rich microcontroller, over-current protective devices, very low-loss GaN-FETs or highly integrated GaN-FET half-bridge gate drivers. In parallel this allows a cost effective and compact PCB design. However, special consideration has to be given to the component selection and design process.

We have presented here a possible component selection process and the associated development approach. The selection of concrete components and design decisions were discussed. Critical functions and their components were identified and potential measures for increasing fault tolerance were presented. These include redundancy mechanisms at board and function level, techniques to cope with the occurrence of latch-ups and transients, as well as planned radiation testing of selected components for qualification. The next steps to increase the TRL of the power stage are radiation tests to qualify the selected most critical components. First of all heavy ion tests supplemented by followed board level tests with proton irradiation are conceivable.
Furthermore, a full performance characterization of the power stage is required to specify peak performances and thermal behaviour.

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